Synthesis of CMOS Gates

Let's consider the design synthesis of CMOS gates by considering the design synthesis of PUN and PDN separately.

PDN Design Synthesis

1. If the PDN is **conducting**, then the **output** will be **low**. Thus, we must find a Boolean expression for the **complemented output** $\overline{Y}$.

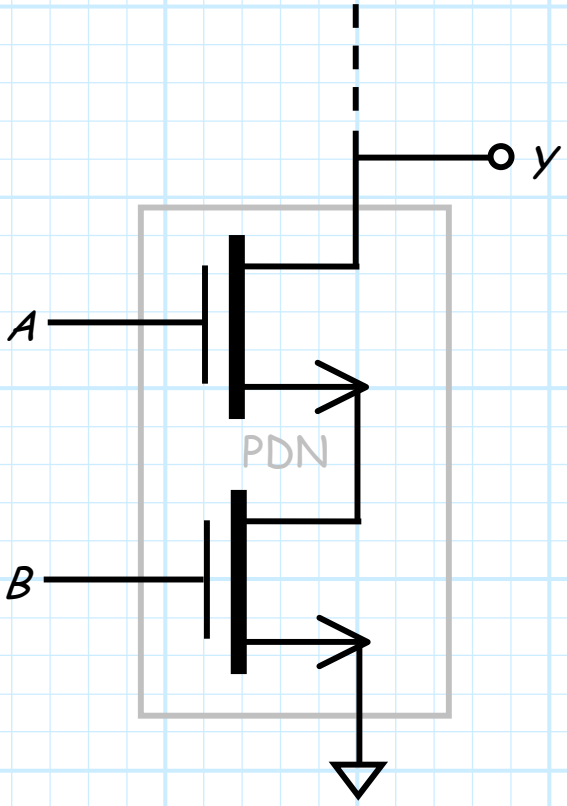
In turn, the PDN can only be conducting **if one or more** of the NMOS devices are **conducting**—and **NMOS** devices will be conducting (i.e., **triode** mode) when the **inputs are high** ($V_{GSN} = V_{DD}$).

Thus, we **must** express $\overline{Y}$ in terms of **un-complemented inputs** A, B, C, etc (i.e., $\overline{Y} = f(A,B,C)$).

e.g., → $\overline{Y} = A + BC$

This step may test our **Boolean algebraic** skills!

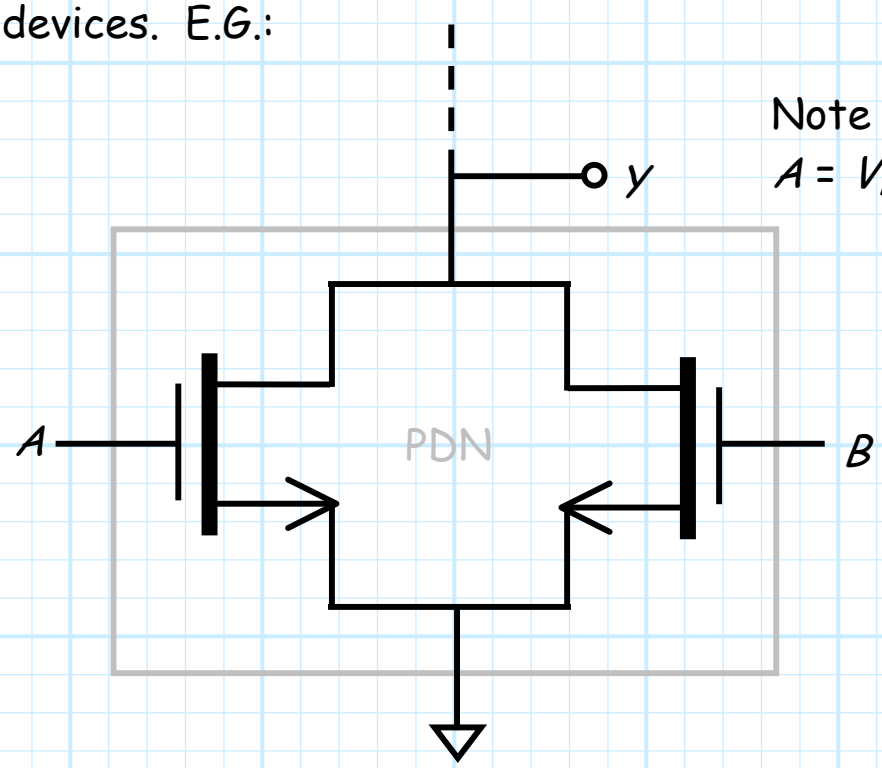
2. Then, we realize **AND** operations in $\overline{Y} = f(A,B,C)$ with **series NMOS** devices. E.G.:



Note that Y=0 if **both** $A = V_{DD}$ **AND** $B = V_{DD}$.

$$\therefore \quad \overline{Y} = AB$$

3. Likewise, we realize **OR** operations with **parallel NMOS** devices. E.G.:



Note that Y=0 if **either** $A = V_{DD}$ **OR** $B = V_{DD}$.

$$\therefore \quad \overline{Y} = A + B$$

PUN Design Synthesis

1. If the PUN is **conducting**, then the **output** will be **high**. Thus, we must find a Boolean expression for the **un-complemented output** Y.

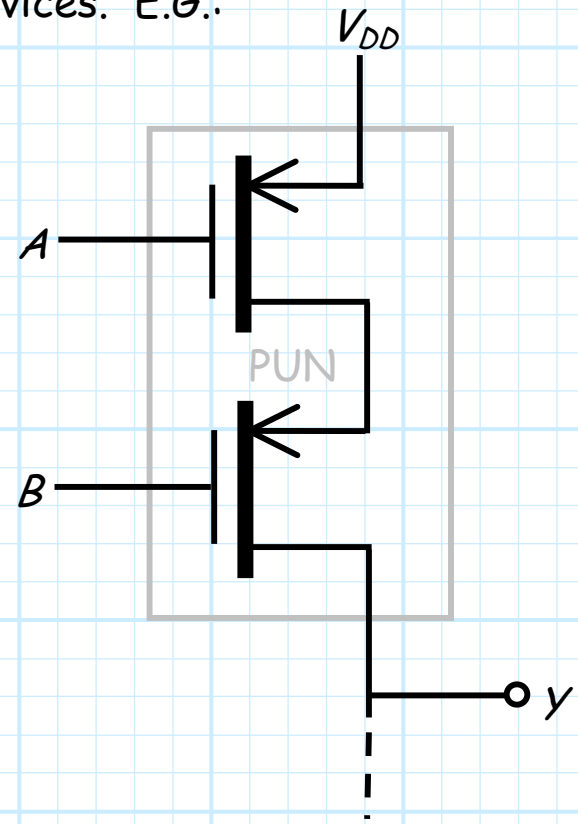
In turn, the PUN can only be conducting **if one or more** of the PMOS devices are **conducting**—and **PMOS** devices will be conducting (i.e., **triode** mode) when the **inputs are low** ($V_{GSP} = -V_{DD}$).

Thus, we **must** express Y in terms of complemented inputs $\overline{A}, \overline{B}, \overline{C}$, etc (i.e., $Y = f\left(\overline{A}, \overline{B}, \overline{C}\right)$).

e.g., → $Y = \overline{A} + \overline{B}\,\overline{C}$

This step may test our **Boolean algebraic** skills!

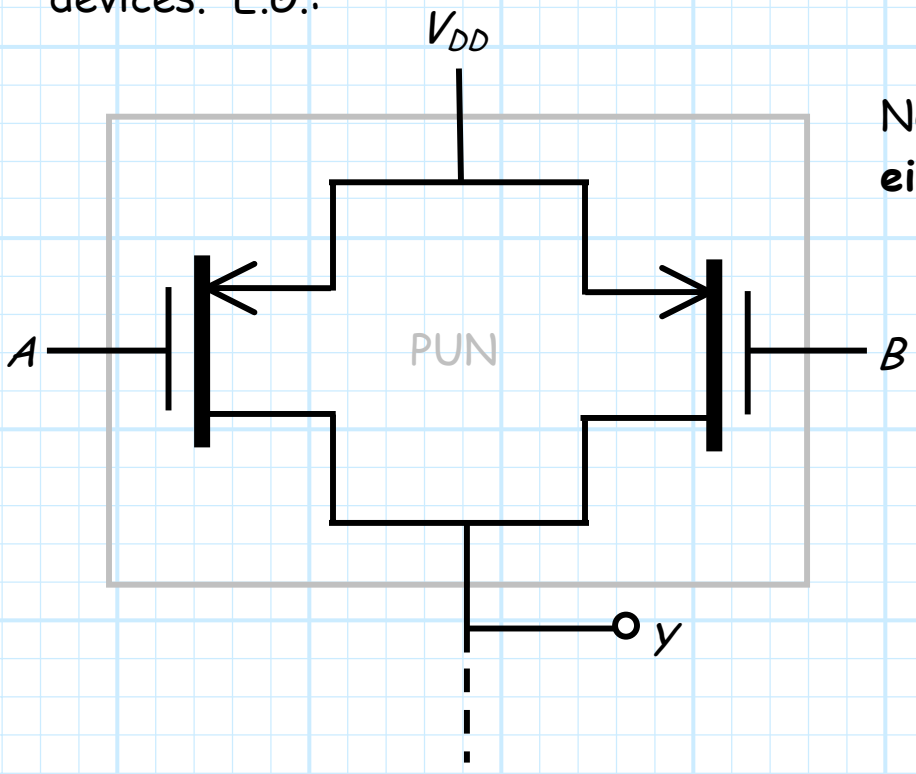
2. Then, we realize **AND** operations with **series PMOS** devices. E.G.:



Note that $Y = V_{DD}$ if **both** $A = 0$ **AND** $B = 0$.

$$\therefore \quad Y = \overline{A}\,\overline{B}$$

3. Likewise, we realize **OR** operations with **parallel PMOS** devices. E.G.:



Note that $Y = V_{DD}$ if **either** $A = 0$ **OR** $B = 0$.

$$\therefore \quad Y = \overline{A} + \overline{B}$$